SYCARD
TECHNOLOGY

PCCtest 450/460
User's Manual

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1.0 Introduction

The PCCtest 450/460 series of PC Card socket testers is designed to provide manufacturers of PC Card based hosts a quick method of testing and verifying the operation of the CardBus, 16-bit and Zoomed Video interface. Sycard's socket testers support PCMCIA's PC Card standard and the Yenta Socket Controller architecture

The PCCtest unit is a Type II PC Card that plugs into a standard Type II or III socket. The test unit is designed for both automated GO/NO-GO testing and component level debug. Test software resides on both the host PC and PCCtest unit. Simple command line invocation allows tests to be embedded into batch test files.

An on-board microcontroller provides the intelligence for the PCCtest unit. The microcontroller is responsible for verifying I/O signals and also provides test stimulus to the PC card socket. The microcontroller can determine the type of error and can even narrow the error down to a specific pin or group of pins.

The PCCtest contains an on-board A/D to provide accurate measurement of VCC and VPP voltages. A digital audio test provides a standard 1KHz tone to test the audio function when the PC Card is configured for I/O mode.

PCCtest is compatible with any Type II or III socket designed to support the PC Card standard. Software included with the PCCtest unit supports a wide variety of socket controllers based on the Yenta socket controller. For other socket controller architectures, Sycard Technology can provide technical documentation describing how to create custom test programs for the PCCtest series of socket testers.

1.1 The PCCtest Models

Sycard Technology supplies two different configurations of the PCCtest 450/460 socket tester for various test and debug needs.

PCCtest 460 - CardBus, PC Card-16 and Zoomed Video socket tester - Replaces the PCCtest 450
PCCtest 450 - CardBus, PC Card-16 and Zoomed Video socket tester - Discontinued

PCCtest 560 - Same as the Model 460 with the addition of a debug serial port. - Replaces the PCCtest 550
PCCtest 550 - Same as the Model 450 with the addition of a debug serial port. - Discontinued

The following table summarizes the various PCCtest models and the feature sets for each:

Model	Support	16-bit	Card Bus	Zoomed Video	Serial Port Debug	Recommended Socket Controllers
450/460	PCMCIA Release 5.x and above	Yes	Yes	Yes	No	Any Yenta Compliant Socket Controller
550/560	PCMCIA Release 5.x and above	Yes	Yes	Yes	Yes	Any Yenta Compliant Socket Controller

Table 1.1-1 PCCtest model matrix

1.2 Compatibility

PCCtest has been designed to be compatible with a wide variety of host socket controllers. Host test software is compatible with most PC compatible machines. The current software supports the following socket controllers:

- Texas Instruments PCI-1130, PCI-1131, PCI1250, PCI1250A, PCI1220, PCI1221, PCI1225, PCI1251A/B

- Texas Instruments PCI1210, PCI1211, PCI1450, PCI1410, PCI1420, PCI4450, PCI4410, PCI1451
- Texas Instruments PCI4451,PCI4410,PCI1520, PCI1620, PCI4510, PCI7510, PCI1510
- Texas Instruments PC7510,PCI1510,PCI7620,PCI6620, PCI7420, PCI6420, PCI7410
- Texas Instruments PCI7x21/7x11/6x21/6x11, PCI6515/x515
- Cirrus Logic CL/PD6832, CL/PD6833
- Cirrus Logic CL/PD6729 and 6730 (16-bit and Zoomed Video only)
- Ricoh RL5C466, RL5C465, RL5C476, RL5C478 and RL5C475
- Ricoh R5C522, R5C551, R5C521, R5C552, R5C554, R5C576A, R5C590, R5C592, R5C593
- Ricoh R5C485,R5C486
- O2 Micro OZ6832, OZ6833, OZ6836, OZ6860, OZ6812, OZ6912, OZ6933
- O2 Micro OZ6922, OZ711EC1/M1, OZ711EC1, OZ711M1, OZ711E2, OZ711M2, OZ711M3
- O2 MicroOZ6933M1, OZ711/MP1/MS1/MP3/MS3/MC1/MC3
- ENE 1225, ENE 1420, ENE 1211, ENE 1410, ENE 710, ENE 720, ENE 714, ENE 724

Support for new socket controllers is always in the works. Contact Sycard or visit their web site at www.sycard.com for the latest list of supported controllers.

1.3 Specifications

Electrical

Supply Voltage	5V ±10%
	3.3V ± 5%
Supply Current	<250mA

Physical

Height	5.0mm
Length	85.6mm
Width	54mm

Environmental

Temperature	0 - 50 degrees C
Humidity	0 - 95 % Non condensing

Reliability

Connector Life Rated at 10,000 insertion/removal cycles (PCMCIA Specification). Actual life is estimated to be 20,000+ cycles.

1.4 Packing List

The PCCtest package includes the following:

- PCCtest 450 or 460 PC Card
- PCCtest 450/460 Test Software Diskette
- PCCtest 450/460 User's Manual
- PCCtest 450/460 Zoomed Video Software User's Manual
- CardBus Configuration Header (deleted with option 01)
- PC Card-16 Configuration Header (deleted with option 01)
- PCCtest 450/460 application notes
- PCCtest 457 switchable Configuration Header (option 01 only)

1.5 Related Documentation

PCMCIA PC Card Specification, Release 2.1
PCMCIA PC Card Specification, February 1995 Release
The PCMCIA Developer's Guide, 3rd Edition - Sycard Technology
Exchangeable Card Architecture (ExCA) release 1.5
Yenta PCI to PCMCIA CardBus Bridge Register Description release 2.2
Texas Instruments PCI1130/PCI1131
Texas Instruments PCI1250/1251/1251B/1450 Datasheet
Texas Instruments PCI1220/1221/1225 Datasheet
Texas Instruments PCI1210/1211/1410/1420 and 4450 Datasheet
Cirrus Logic CL-PD6832 Datasheet
Ricoh RF5C466, RF5C465, RF5C476, RF5C478 Datasheets
Ricoh R5C476M2, R5C478M2, R5C521/522/551/552/554/576A/590/592/593 Datasheets
O2 Micro 6832,6833,6836,6812,6860,6933 and 6912 Datasheets
O2 Micro 711EC1/711M1/711E2/711M2/711M3/6933E Datasheets

1.6 Installing the PCCtest Software for 16-bit and CardBus Testing

The PCCtest software consists of an executable program. PCT450.EXE is the executable for testing the 16-bit portion of the interface. TESTCB.EXE is the executable for CardBus (32-bit) testing.

To install the PCCtest software simply copy the PCT450.EXE or TESTCB.EXE to your hard disk. Both programs may also be executed directly from the floppy disk. Also included on the diskette is a READ.ME file containing information on any recent changes in the PCCtest software.

PCCtest software updates, application notes and user manuals are always available on the Sycard Technology WEB site at ***http://www.sycard.com/support.html***. Technical Q&A, common problems and Beta test software can be found at ***http://www.sycard.com/tech450.html***. For technical support contact Sycard Technology via email at **support@sycard.com**.

Zoomed Video test software is included on the same diskette. A description of the Zoomed Video software may be found in the **PCCtest 450/460 Zoomed Video Software User's Manual** included with the PCCtest 450.

1.7 PCCtest 450/550 Revisions

There are currently three revisions of PCCtest 450 and one revision of the PCCtest 460 in the field. Later versions of the PCCtest 450 support more socket controllers. Older revisions of the PCCtest 450 are factory upgradeable. Contact Sycard Technology for upgrade details and pricing.

Revision	Socket Controller Support
1.00	TI PCI1130
1.01/1.02*	TI PCI1130/1131, Cirrus 6832
1.03/1.04*	TI PCI1130/1131/1250, Cirrus 6832, Ricoh RL5C466/465/476/478
1.05/1.06*	All CardBus controllers

PCCtest 450 and 550 Revisions

Notes: * Second revision number refers to PCCtest 550.
** For TI PCI12xx, 14xx, 44xx, 16xx, 45xx, 15xx, and 75xx support, see appendix C.

1.8 PCCtest 460/560 Revisions

The PCCtest 460 and 560 are functionally equivalent to the PCCtest 450 and 550. The PCCtest 460/560 were created because a key component used in the PCCtest 450/550 was being discontinued. The 460/560 was designed to replace the 450/550 and not add any new features or improve performance.

Revision	Socket Controller Support
1.05/1.06	TI PCI1130/1131/12xx/14xx/44xx, Ricoh RL5C466/465/476/478, Cirrus 6832, O2 OZ6832++, OZ6836++, OZ6833, OZ6812, OZ69xx
1.06/1.07	TI PCI 7510 and newer TI controllers

PCCtest 460 and 560 Revisions

Notes: * Second revision number refers to PCCtest 560.
** For TI PCI12xx, 14xx, 44xx, 16xx, 45xx, 15xx, and 75xx support, see appendix C.

2.0. PCCtest Operation

The procedure for testing the desired socket is simple. Inserting the PCCtest 450/460 unit into the socket, connect the appropriate configuration header and invoke the one of the test programs. The test program will execute a variety of tests automatically and return PASS or FAIL status. If any errors are detected, they will be displayed on the screen.

> ***Note:*** *The PCCtest will not operate correctly with Socket and Card Services present. Remove all PCMCIA driver software from AUTOEXEC.BAT or CONFIG.SYS files and re-boot before using PCCtest.*

2.1 32-bit PCCtest Software

Syntax

```
TESTCB -0 -1 -ax -cx -bxx -h -jxxxx -lx -nxxx -p -q -sx -v -w -m
```

Switches

-0	Test socket 0
-1	Test socket 1
-ax	PCIC Controller address select -a1 = 3E2-3E3H, -a2 = 3E4-3E5H, -a3 = 3E8-3E9H
-bxx	Select Socket controller xx = Socket controller See help menu in section 2.21 for supported socket controllers
-cx	Use PCCtest 455 external Control unit - default = LPT1, x = 2 = LPT2, 3 = LPT3
-d	Use PCI BIOS to access PCCtest configuration space
-h	No Vcc test
-lx	Long power on delay (x = integer 1-32768)
-m$	Debug Menu
-mx:y	Test Options
-nxxx	Select alternate I/O window address (default = 150H)
-jsxxxx	Select alternate memory window address in lower 1Mbyte address space (default = D000:F - DFFF:F)
-jLyyyyyyyy	Select alternate memory window address in 32-bit address space
-kx	Select alternate PCI Bus # for PCCtest, SLOT 0 = x, SLOT 1 = x+1
-q	Quiet mode - Disables speaker test
-sx	CardBus Chip number, s2 = 2nd CardBus controller, s3 = 3rd CardBus controller
-kx	PCI Bus number for slot 0. (Default = PCI Bus 2 for slot 0 and PCI Bus 3 for slot 1)
-t	Enable Vpp measurement with 10% tolerance
-tx	Enable Vpp measurements with x% tolerance on Vpp measurements (-t7 = 7% tolerance)
-v	Verbose mode. Displays test progress and error messages
-w	10% tolerance on Vcc measurements
-wx	x% tolerance on Vcc measurements (-w7 = 7% tolerance)

*Note: ** For additional notes on TI and ENE controllers, see Appendix C*

Note: Executing TESTCB without options displays a help menu with a list of currently supported socket controllers

2.1.1 Using the 32-bit PCCtest Software

The following example illustrates how to test a Texas Instruments PCI-1250A CardBus controller in 32 mode:

```
TESTCB -b65B -v -1<CR>

PCCtest 450/460 CardBus test software v2.10
Texas Instruments PCI-1250A on Bus  0, Function  0, Device  3, Controller 1
Current Slot = 0  Scratch Buffer = 33BF:0000
CardBus Socket Registers = 000D8000  Test Memory Window = 000D4000  CBus =  1
Checking Socket Controller..............Passed
Power on delay (Vcc = 3.3 volt).........Complete
Basic Operational Test..................Passed
Data Pattern Test.......................Passed
Parity Error Test (CPERR#)..............Passed
Parity Test (CPAR)......................Passed
CSERR# Test.............................Passed
Vcc Test................................Passed
Speaker Test............................Passed
CSTSCHG Test............................Passed
CINT# Test..............................Passed
CRST# Test..............................Passed
CCLKRUN# Test...........................Passed
Slave Abort (CSTOP#) Test...............Passed
PCCtest model number 460  - Version 1.07
Configuring PCCtest Master Mode (M1).....Complete
Master Mode Read Test...................Passed
Master Mode Write Test..................Passed
Test completed with 0 errors - PASSED
```

Note: The "B" added to the "-b65" specifies that the TESTCB software configures the PCI1250/1250A to generate the clock for the voltage switch. See Appendix C for a more detailed explanation of this switch.

2.1.1 Using the 32-Bit PCCtest Software

Section 2.1 describes the command line switches used to invoke the 32-bit PCCtest software. If a manual is not handy, the PCCtest software includes a single screen listing of the command line switches. To view this screen, simply enter the TESTCB command without any switches:

```
Sycard Technology PCCtest 450/460 CardBus test software v2.10
 PCCtest Help Menu - Page 1/3 Command Line Switches
  -0  Select socket 0
  -1  Select socket 1
  -v  Verbose - display tests progress
  -q  Disable Speaker test
  -sx PCI Chip Number -s2 = 2nd CardBus controller
  -tx Enable Vpp testing with 10% tol  -t11 = 11% tolerance
  -wx Vcc tolerance (default=5%), -w10 = 10% tolerance
  -lx Long power cycle delay (x = timer ticks)
  -jsxxxx Alt DOS mem segment (xxxx = segment D000:0 - D3FF:F default)
  -jLyyyyyyyy Alt long mem address (yyyyyyyy = 32 bit address)
  -nxxxx Alt I/O addr (150H default)
  -cx  Use External control unit x=LPT port
  -d  Use PCI BIOS to access PCCtest Config Space
  -kx Select alt PCI Bus # for PCCtest SLOT0=x SLOT1=x+1
  -m$ Enter debug menu              -mx:y Test options
```

```
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       Hit any key for next page, ESC to exit help menu...Sycard Technology
```

Page 2 Help

```
PCCtest 450/460 CardBus test software v2.10
 PCCtest Help Menu - Page 2/3 Supported Socket Controllers
  -bxy  Select chip type
   -b10 - Cirrus CL/PD6832        -b12 - Cirrus CL/PD6833

   -b40 - Ricoh 5C466      -b41 - Ricoh 5C465      -b42 - Ricoh 5C476
   -b43 - Ricoh 5C478      -b44 - Ricoh 5C475      -b45 - Ricoh 5C475M2
   -b46 - Ricoh 5C476M2    -b47 - Ricoh 5C478M2    -b45 - Ricoh R5C521
   -b46 - Ricoh R5C522     -b45 - Ricoh R5C551     -b46 - Ricoh R5C552
   -b46 - Ricoh R5C554     -b46 - Ricoh R5C576A    -b46 - Ricoh R5C590
   -b46 - Ricoh R5C592     -b46 - Ricoh R5C593     -b45 – Ricoh R5C485
   -b46 – Ricoh R5C486

   -b60    - TI PCI1130    -b61    - TI PCI1131    -b62(b) - TI PCI1250
   -b63(b) - TI PCI1220    -b65(b) - TI PCI1250A   -b67(b) - TI PCI1221
   -b68(b) - TI PCI1210    -b69(b) - TI PCI1225    -b70(b) - TI PCI1251A
   -b71(b) - TI PCI1450    -b72(b) - TI PCI1211    -b73(b) - TI PCI1251B
   -b74(b) - TI PCI4450    -b75(b) - TI PCI1420    -b76(b) - TI PCI1410
   -b77(b) - TI PCI1451    -b78(b) - TI PCI4451    -b79(b) - TI PCI4410
   -b80(b) - TI PCI1520    -b82(b) - TI PCI1620    -b83(b) - TI PCI4510
   -b84(b) - TI PCI7510    -b85(b) - TI PCI1510    -b86(b) - TI PCI7620/6620
   -b87(b) - PCI7420/6420  -bb0(b) - PCI7410  -bb1 - PCI7x21/7x11/6x21/6x11
   -bb2(b) - PCI6515/x515
      Add b suffix to TI Controllers to enable voltage switch clock

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```

Page 3 Help

```
PCCtest 450/460 CardBus test software v2.10
 PCCtest Help Menu - Page 3/3 Supported Socket Controllers
  -bxy  Select chip type
   -b50 - O2 OZ6832C       -b52 - O2 OZ6836C       -b53 - O2 OZ6833
   -b54 - O2 OZ6860        -b55 - O2 OZ6812        -b56 - O2 OZ6933/711E1
   -b57 - O2 OZ6912/711E0/601  -b58 - O2 OZ6922    -b59 - O2 OZ711EC1/M1
   -b5a - O2 OZ711EC1      -b5b - O2 OZ711M1/MC1   -b5c - O2 OZ711E2
   -b5d - O2 OZ711M2       -b5e - O2 OZ711M3/MC3   -b5f - O2 OZ6933E
   -bd0 - O2 OZ711MP1/MS1  -bd1 - O2 OZ711MP3/MS3

   -b91(b)-ENE 1225        -b92(b)-ENE 1420        -b93(b)-ENE 1211
   -b94(b)-ENE 1410        -b95(b)-ENE 710         -b96(b)-ENE 720
   -b97(b)-ENE 714         -b98(b)-ENE 724

  Add b suffix to ENE 12xx/14xx/7xx to enable voltage switch clock

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```



```
Hit any key for next page, ESC to exit help menu...
```

***Note**: Before the TESTCB software can be run, the CardBus I/O configuration header must be connected to the PCCtest 450/460 card.*

2.2 16-Bit PCCtest Software

The PCCtest software is a MS-DOS application distributed on a single floppy diskette. Included on the diskette is the test application program (PCT450.EXE), and a READ.ME file containing information not contained in this document. The PCCtest program has the following run time switches:

Syntax

```
PCT450 -0 -1 -a -bxx -c -gx -h -i -jxxxx -lx -nxxx -p -q -sx -t -v -w -yx
```

Switches

-0 Test socket 0 - primary socket controller at base address 3E0-3E1H
-1 Test socket 1 - primary socket controller at base address 3E0-3E1H
-ax PCIC Controller address select -a1 = 3E2-3E3H, -a2 = 3E3-3E4H, -a3 = 3E5-3E6H
-bxx Select Socket controller xx = Socket controller
See section 2.2.2 for list of selected socket controllers
-c Select common Vpp (Vpp1 = Vpp2)
-gx Test Vcc select
-g3 = Test at Vcc = 3.3 volts, -g5 = Test at Vcc = 5.0 volts (default), -ga = Test at Vcc = 3.3/5V
-hx -h0 = Bypass Vcc and Vpp tests, -h1 = Bypass Vpp test, -h2 = Bypass Vcc test,
h3 = Bypass Vpp 12V test
-j(s)x Select alternate memory window. -j1 = C800:0 - CFFF:0, -j2 = E000:0 - E7FF:0
-jsxxxx = specify memory segment in lower 1Mbyte, example jsB800 selects B800:0 window
-jLyyyyyyyy = specify 32-bit memory address, example jL50000000 selects 50000000H window
-lx Long power on delay (x = integer 1-32768)
-nxxx Select alternate I/O window address (default = 150H)
-p 5V / 12V Vpp.
-q Quiet mode - Disables speaker test
-tx x% tolerance on Vpp measurements (default = 5%).
-v Verbose mode. Displays test progress and error messages
-wx x% tolerance on Vcc measurements (default = 5%)
-yx Select PCCtest 455 external control unit LPT port. -y2 = LPT2, -y3 = LPT3

***Note:** Switches can be entered in any order and must be separated by a space.*
***Note:** ** For additional notes on TI and ENE controllers support, see Appendix C*

2.2.1 PCCtest Host Software Environment

The PCCtest software is designed to run under DOS 3.0 or higher. During the test PCCtest software makes direct I/O and memory accesses to PCCtest resources. Any software or operating system that blocks or allocates resources that conflicts with the PCCtest software will cause the test to fail. See section 3.0 for information on the resources used by the PCCtest software.

In Windows 95/98 the PCCtest software should be run in a MSDOS Safe mode. This assures that sufficient upper memory areas are available for the test windows. Operation in a “DOS Box” under windows is not recommended. To enable a Safe mode DOS environment, reboot the computer and enter <F8> as the computer starts to boot. A user can select a MSDOS Safe Mode from the startup menu.

2.2.2 Using the 16-bit PCCtest Software

Section 2.2 describes the command line switches used to invoke the 16-bit PCCtest software. If a manual is not handy, the PCCtest software includes a two-screen listing of the command line switches. To view this screen, simply enter the PCT450 command without any switches:

PCT450<CR>

```
Sycard Technology PCCtest 450/460 16 Bit Software v1.22  m d b t
 PCCtest Help Menu - Page 1/3 Command Line Switches
  -0   Select socket 0                -nxxx Alternate I/O Address
  -1   Select socket 1                -p    5V/12V Vpp
  -2   Select socket 2                -q    Disable Speaker Test
  -3   Select socket 3                -r    Not Used
  -ax  Socket Controller base addr    -sx   PCI Chip Number
    a1=3E2,a2=3E4,a3=3E8,a4=3E6       -tx   x% Vpp Tolerance  def=5%
  -bxx Select Chip Type               -u    Not Used
  -c   Common Vpp1 and Vpp2           -v    Verbose - Show Errors
  -g   Select Test Voltage            -wx   x% Vcc Tolerance  def=5%
        g3=3.3V, g5=5V, -ga=Both      -x    Not Used
  -h   Disable all Voltage Tests      -yx   PCCtest 455 LPT Port
        h1-No Vpp Test, h2-No Vcc Test      -y2 = LPT2, -y3 = LPT3
        h3-No Vpp 12V Test
  -jx  Mem window 1=C800, 2=E000      -m$   Enter debug menu
        jsxxxx Select Segment xxxx    -mx:y Test options
        jLyyyyyyyy Select 32 bit address use with -am
  -lx  Long power-on delay




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```

Page 2 of help menu

```
Sycard Technology PCCtest 450/460 16 Bit Software v1.22
 PCCtest Help Menu - Page 2/3 Supported Socket Controllers

  -bxy  Select chip type
   -b42 - Ricoh RF5C466     -b43 - Ricoh RF5C465    -b44 - Ricoh 5C476/476M2
   -b45 - Ricoh 5C478/478M2 -b46 - Ricoh 5C475/475A -b46 - Ricoh R5C521
   -b45 - Ricoh R5C522      -b46 - Ricoh R5C551     -b44 - Ricoh R5C552
   -b44 - Ricoh R5C554      -b44 - Ricoh R5C576A    -b44 - Ricoh R5C590
```



```
   -b44 - Ricoh R5C592      -b44 - Ricoh R5C593     -b46 – Ricoh R5C485
   -b44 – Ricoh R5C486
   -b62    - TI PCI1130     -b63    - TI PCI1131    -b64    - TI PCI1031
   -b65(b) - TI PC1250A     -b66(b) - TI PCI1220    -b67(b) - TI PCI1221
   -b68(b) - TI PCI1210     -b69(b) - TI PCI1225    -b70(b) - TI PCI1251A
   -b71(b) - TI PCI1450     -b72(b) - TI PCI1211    -b73(b) - TI PCI1251B
   -b74(b) - TI PCI4450     -b75(b) - TI PCI1420    -b76(b) - TI PCI1410
   -b77(b) - TI PCI1451     -b78(b) - TI PCI4451    -b79(b) - TI PCI4410
   -b80(b) - TI PCI1520     -b82(b) - TI PCI1620    -b83(b) - TI PCI4510
   -b84(b) - TI PCI7510     -b85(b) - TI PCI1510    -b86(b) - TI PCI7620/6620
   -b87(b) - TI PCI7420/6420 -bb0(b) - TI PCI7410
   -bb1-TI PCI7x21/7x11/6x21/6x11   -bb2-TI PCI6515/x515
  Note:  PC Card-16 Configuration header must be used
  TI PCI12xx,14xx,44xx,15xx,45xx series, 'b' suffix for ext volt switch clock

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```

Page 3 of help menu

```
Sycard Technology PCCtest 450/460 16 Bit Software v1.22
 PCCtest Help Menu - Page 3/3 Supported Socket Controllers

  -bxy  Select chip type
   -b12 - Cirrus CL/PD6729        -b13 - Cirrus CL/PD6730
   -b14 - Cirrus CL/PD6832        -b16 - Cirrus CL/PD6833

   -ba0-O2 OZ6832C  -ba2-O2 OZ6836C     -ba3-O2 OZ6860      -ba4-O2 OZ6833
   -ba5-O2 OZ6812   -ba6-O2 OZ6933      -ba7-O2 OZ6912/711E0/601 -ba8-O2 OZ6922
   -ba6-O2 OZ711E1  -ba9-O2 OZ711EC1/M1 -baa-O2 OZ711EC1    -bab-O2 OZ711M1/MC1
   -bac-O2 OZ711E2  -bad-O2 OZ711M2     -bae-O2 OZ711M3/MC3 -baf-O2 OZ6933E
   -bd0-O2 OZ711MP1/MS1  -bd1-O2 OZ711MP3/MS3

   -bc0(b)-ENE 1225 -bc1(b)-ENE 1420 -bc2(b)-ENE 1211 -bc3(b)-ENE 1410
   -bc5-ENE 710     -bc6-ENE 720        -bc7-ENE 714         -bc8-ENE 724



  Note:  PC Card-16 Configuration header must be used
  ENE 12xx,14xx,7xx, 'b' suffix for ext volt switch clock

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```

> ***Note**: Before using the PCCtest 450/460 to test the 16-bit portion of the interface insure the PC-Card 16 Configuration header is plugged into the PCCtest's 15 pin I/O connector.*

Before attempting to test the PC Card socket, the user must first determine several parameters about their socket. The first item to determine is the vendor and part number of the socket controller. Verify that the socket controller is supported in the list shown in the help screen. If the part is not listed, call Sycard Technology for testing information. The second step is to start building the command line string used to invoke the PCCtest software. The user must specify the slot number, the various test options and display options. For example, when testing the TI PCI1130 the following command line is used. This command line will test slot 1 of the Texas Instruments PCI1130 and display the test progress and all errors.

```
PCT450 -b62 -v -1 -c<CR>

Sycard Technology PCCtest 450/460 16-bit Software v1.22
Looking for Texas Instruments PCI-1130 PCI Controller #0...
Testing Slot 1   I/O base = 150H   Memory Window = D000:0
Socket Controller = Texas Instruments PCI-1130
Checking Socket Controller..............Passed
Power on delay (Vcc = 5 volt)............Complete
Basic operational test..................Passed
Data pattern test.......................Passed
Address pattern test....................Passed
Status bit pattern test.................Passed
Wait bit test...........................Passed
Reset test..............................Passed
Card voltage test.......................Passed
Audio out test..........................Complete
Test completed with 0 errors - PASSED
```

Example 1 - Testing the Texas Instruments PCI-1250A

The TI PCI-1250A is a single chip, dual socket CardBus PC Card controller. The PCI-1250/1250A follows the recommendations of the Yenta Specification. The following examples illustrate various command line options used to test the various system implementation of the PCI-1250/1250A.

1. GO/NO-GO test of slot 0 of a dual slot portable computer using the PCI-1250/1250A. The following command line will execute the test on slot 0 and suppress error listings. A final Pass/Fail message will be output after the test is complete.

```
PCT450 -0 -b65B -v

Sycard Technology PCCtest 450/460 16-bit Software v1.22
Looking for Texas Instruments PCI-1250A PCI Controller #0...
Testing Slot 0   I/O base = 150H   Memory Window = D000:0
Socket Controller = Texas Instruments PCI-1250A
Test completed with 0 errors - PASSED
```

Note: *The "B" added to the "-b65" specifies that the PCT450 software configures the PCI1250/1250A to generate the clock for the voltage switch. See appendix C for a more detailed explanation of this switch.*

Example 2 - Embedding PCT450.EXE in a Batch File

PCT450.EXE can be embedded in a batch file or called from a test executive. The following illustrates a batch file that will continue to test socket 0 until a failure is detected.

```
echo off
:loop
PCT450 -0 -b11 -v
if errorlevel 1 goto exit
goto loop
:exit
echo on
```


3.0 Hardware Notes

The PCT450 and TESTCB software is designed to test socket controllers based on Intel's Yenta PCI to PCMCIA CardBus bridge register description. All tests require certain I/O and memory resources. These resources are listed in the following table:

Application	Slot 0	Slot 1
TESTCB.EXE Version 2.05 and later	D000:0 – D0FF:F D200:0 – D2FF:F 160H – 16FH PCI Bus 2	D100:0 – D1FF:F D300:0 – D3FF:F 150H – 15FH PCI Bus 3
PCT450.EXE	D000:0 - D000:7FFF – Memory 150H – 15FH – I/O	D000:0 - D000:7FFF – Memory 150H – 15FH – I/O
ZVTEST.EXE	D000:0 – D000:7FFF – Memory 150H – 15FH – I/O	D000:0 – D000:7FFF – Memory 150H – 15FH – I/O

Table 3..0-1 PCCtest System Resource Requirements

3.0.1 32-Bit Testing Resource

The TESTCB software requires I/O resources at 150H to 15FH for testing slot 0 and 160H to 16FH for testing slot 1. Memory resources at D000:0 to D3FF:F are used to map the PCCtest's memory space and also socket controller resources. The **-jsxxxx** allows the user to select an alternate base address for this memory window in the lower 1Mbyte address space. If there are no resources available in the lower 1Mbyte address space, the user may specify a 32-bit address with **–jLyyyyyyyy** option. For example to use PCI address E7000000 use –jLE7000000.

The TESTCB software will also assign slot 0 to PCI Bus 2 and slot 1 to PCI Bus 3 during the duration of the test. In a system with multiple PCI buses, the user may need to select an alternate PCI bus for CardBus testing. The **–kx** option allows the user to select which PCI bus number is assigned to slot 0 and slot 1.

3.0.2 16-Bit Testing Resource

The PCT450 software requires certain I/O and memory address space resources to carry out its test. For the full duration of the test, the PCCtest program will open up an I/O window at 150-15FH. The **-nxxx** option allows the user to specify an alternate 16-byte I/O window. In addition, a 32K byte memory window at D000:0 - D7FF:F is used for common and attribute memory testing. The **-jsxxxx** allows the user to select an alternate base address for this memory window in the lower 1Mbyte address space. If there are no resources available in the lower 1Mbyte address space, the user may specify a 32-bit address with **–jLyyyyyyyy** option. As a default all ExCA registers are accessed via the standard 3E0/3E1 I/O address space. To specify that these registers are memory mapped, use the **–am** option

For example to use PCI address E7000000 and have the ExCA registers memory mapped use the following:

-jLE7000000 -am

3.1 Using the PCCtest 455 External Control Unit

The PCCtest 455 external control unit is an optional accessory designed to facilitate the testing of the different modes of the CardBus socket. Without the PCCtest 455 the user must manually change the configuration headers when switching between CardBus and PC Card-16 mode. The PCCtest 455 allows for program control of the Card Detects and Voltage sense pins. Enclosed in an external enclosure, the PCCtest 455 interfaces between the host system's parallel port and the PCCtest's 15 pin I/O connector. All PCCtest 450/460 software programs include support for the PCCtest 455. The following table lists the command line switch to select which parallel port is used for PCCtest 455 control.

Program	PCCtest 455 Option
TESTCB.EXE	-cx
PCT450.EXE	-yx
ZVTEST.EXE	-yx

Table 3.1-1 Supporting the PCCtest 455

***Note**: x denotes which parallel port is used to interface to the PCCtest 455. For example -c1 selects LPT1 and -c2 selects LPT2.*

3.2 PCCtest Revisions

The following table describes the released versions of the PCCtest hardware. The revision identification is located on the serial number label of the PCCtest unit.

Model	Rev	Description
PCCtest 450	1.00	Initial release of PCCtest 450. Support TI PCI1130, PCI1131 and Cirrus 6832.
PCCtest 450	1.01	Second release of PCCtest 450. Added support for Ricoh RL5C466
PCCtest 450	1.03	Third release of PCCtest 450. Added support for higher performance controllers including TI PCI1250, Ricoh RL5C475 and RL5C465.
PCCtest 450	1.05	Fourth release of PCCtest 450. Added support for TI PCI1250A, PCI1220, PCI1221 and PCI1210
PCCtest 450F	1.05	Flash upgradable version of the PCCtest 450 revision 1.05
PCCtest 460F	1.05	Replacement for the PCCtest 450F
PCCtest 460F	1.07	Second release of the PCCtest 460F with support for TI PCI75xx controllers
PCCtest 550	1.02	Initial release of PCCtest 550, same characteristics as 1.01 release of PCCtest 450.
PCCtest 550	1.04	Second release of PCCtest 550, same characteristics as 1.03 release of PCCtest 450
PCCtest 550	1.06	Third release of PCCtest 550, same characteristics as 1.05 release of PCCtest 450
PCCtest 560F	1.06	Replacement for the PCCtest 550
PCCtest 560F	1.08	Second release of the PCCtest 560F with support for TI PCI75xx controllers

The latest version of the PCCtest software will work with all versions of the PCCtest hardware.

4.0 Test Coverage

PCCtest is designed to provide high test coverage of the PC Card interface. This section will detail the test procedure used to test the PC Card interface and provide information on the test coverage.

4.1 Test Subsections – 32-Bit Tests

The TESTCB.EXE software is designed to verify the 32-bit portion of the PC Card interface. The first steps in the test involve determining the test environment.

1. Verify the presence of a valid PCI BIOS
2. Search for selected socket controller
3. Initialize socket controller

If all of these steps pass, then the test will continue with the Socket Controller test.

4.1.1 Socket Controller Test

The Socket Controller test verifies the interface between the PCI bus and the socket controller chip. A simple data pattern test is run on one of the R/W registers within the socket controller chip. The socket controller test is run before any power is applied to the PC Card socket.

4.1.2 Power On

The test software will attempt to detect that the PCCtest unit is correctly installed in the selected socket. Once the software detects that a valid CardBus card (PCCtest 450/460) is installed, it will attempt to power the slot. The software will command the socket controller to apply 3.3V power to the slot and verify that the socket controller returned status that valid power has been applied.

4.1.3 Data Pattern Test

The Data Pattern Test verifies the data path between the host socket controller and the PCCtest 450/460. Several types of patterns are read and written to the card to verify all 32 address/data signals.

4.1.4 Parity Error Test (CPERR#)

CPERR# is tested by commanding the PCCtest unit to assert CPERR# and making accesses to the PCCtest unit. The test software will verify that CPERR# is detected by reading the CardBus status register located in the socket controller's PCI configuration space.

4.1.5 Parity Test (CPAR)

CPAR is tested by commanding the PCCtest unit to force CPAR to a zero and making accesses to the PCCtest unit. The test software will verify that bad parity is detected by reading the CardBus status register located in the socket controller's PCI configuration space.

4.1.6 CSERR# Test

CSERR# is tested by commanding the PCCtest unit to assert CSERR# and making accesses to the PCCtest unit. The test software will verify that CSERR# is detected by reading the CardBus status register located in the socket controller's PCI configuration space.

4.1.7 Vcc and Vpp Tests

Vcc and Vpp are measured using the PCCtest's internal A/D converter. The test software will verify that Vcc is within 5% of 3.3V. Using the -wx option, the user may specify the tolerance of the Vcc measurements. In normal operation, Vpp is not measured in the TESTCB software. Vpp tests are usually made in the PCT450 software. However, in TESTCB the user may enable Vpp testing with the -tx option. With "x" being the tolerance. When enabled software verifies if Vpp can be switched from Ground, Vcc and 12V.

4.1.8 Speaker Test

The Speaker Test will test the audio capabilities of the CardBus interface. A 1 second 1KHz tone will be output to the host's speaker circuit.

4.1.9 CSTSCHG Test

CSTSCHG is tested by commanding the PCCtest unit to assert CSTSCHG. The test software will verify that CSTSCHG is asserted by reading the Present State Register in the CardBus socket register.

4.1.10 CINT# Test

CINT# is tested by commanding the PCCtest unit to assert CINT#. The test software will verify that CINT# is asserted by reading the Present State Register in the CardBus socket register.

4.1.11 CRST# Test

CRST# is tested by commanding the PCCtest to latch a transition on the CRST# signal. The test software will toggle CRST# and verify that the PCCtest unit detected a transition.

4.1.12 CCLKRUN# Test

CCLKRUN# is tested by commanding the PCCtest to latch a transition on the CCLKRUN# signal. The test software will toggle CCLKRUN# and verify that the PCCtest unit detected a transition.

4.1.13 Slave Abort Test

The slave abort test verifies the operation of the CSTOP# signal. The PCCtest is commanded to respond to a single cycle with a Slave Abort sequence. If the host socket controller detects a slave abort, this verifies the operation of the CSTOP# signal.

4.1.14 Master Mode Read Test

The Master Mode Read test verifies that the PCCtest can initiate a Master Read cycle. A walking one pattern verifies the data bus.

4.1.15 Master Mode Write Test

The Master Mode Write test verifies that the PCCtest can initiate a Master Write cycle. A walking one pattern verifies the data bus.

4.2 Test Subsections - 16-bit Tests

The PCCtest software is designed to run under a DOS environment in a PC architecture machine. A simple command line invocation starts the PCCtest software. Several command line options configure the test for host options. The following output illustrates the test flow for the PCCtest software.

```
Sycard Technology PCCtest 450/460 16-bit Software v1.22
Looking for Texas Instruments PCI-1130 PCI Controller #0...
Testing Slot 1   I/O base = 150H   Memory Window = D000:0
Socket Controller = Texas Instruments PCI-1130
Checking Socket Controller..............Passed
Power on delay (Vcc = 5 volt)...........Complete
Basic operational test..................Passed
Data pattern test.......................Passed
Address pattern test....................Passed
Status bit pattern test.................Passed
Wait bit test...........................Passed
Reset test..............................Passed
Card voltage test.......................Passed
Audio out test..........................Complete
Test completed with 0 errors - PASSED
```

The following sections will describe the tests performed in each test module.

4.2.1 Socket Controller Verification - Test 1

The Socket Controller verification test is intended to provide a basic read/write test of the socket controller's registers. 8 bit read/write tests with all data patterns and verifies the connection of the data bus, system I/O read and write strobes and addressing required to access the socket controllers registers. This test is not designed to test the functionality of the socket controller, but only to verify sufficient operation to continue the test of the socket interface. If this test fails, it indicates that communication between the systems and socket controller's registers and no further testing is possible.

4.2.2 Basic Operational Test - Test 2

The first part of the Basic Operational test verifies that after a power-on delay, card detects are active. If CD1# and CD2# are not low, then the card is not inserted or the card slot is not powered and further testing is not possible. Once card detects are active the Basic Operational Test tests basic read/write functionality of the interface. This test insures that the PC Card interface has enough functionality to continue with the reset of the tests.

1. 8 bit I/O write/read test with the following patterns - 00H, AAH, 55H,5AH,FFH and 11H.
2. 16-bit I/O write/read test with the following patterns - 0000H, AAAAH, AA55H, 55AAH, FFFFH and 1234H.
3. 16-bit memory write/read test with the following patterns - 0000H, AAAAH,AA55H, 55AAH, FFFFH and 1234H.
4. Memory - I/O transfer test - Verifies that a pattern can be written via a memory write and read back via an I/O read. This test will verify if EMS or other memory is mapped to the PC Card memory window. If an error occurs, a message similar to the following will be returned:
   ERROR! - Check EMS or other high memory conflict.

4.2.3 Data Pattern Test - Test 3

The Data Pattern Test is designed to test a full range of data patterns.

a. Walking 1 pattern
b. Walking 0 pattern
c. 64K patterns.

4.2.4 Address Pattern Test - Test 4

The Address Pattern Test utilizes the PCCtest's address latches. Addresses are latched on the PCCtest's on-board address latches and read back and compared with the address accessed. All 26 address and the REG# signal are latched. The address test consists of the following:

a. Walking 1 pattern
b. Walking 0 pattern
c. 64K patterns on lower address lines
d. 64K patterns on upper address lines

4.2.5 Status Bit Pattern Test - Test 5

Status bit pattern test is designed to test the following status bits:

BVD1/STSCNG#
BVD2/SPKR#
WP/IOIS16#
READY/IREQ#

A series of patterns is setup on the PCCtest's output latch and read back through the socket controller's status register.

4.2.6 Wait Bit Test - Test 6

The Wait Bit Test tests the WAIT# signal. WAIT# is tested for both I/O and memory accesses. Utilizing the PCCtest's timing measurement circuit, the PCCtest program will measure the duration of a zero wait state I/O and memory read. The socket controller's wait state generator is setup to add 700ns of wait states. The measurement circuit is armed and both I/O and memory strobes are measured with the added wait states and compared to the zero wait state access. If wait states are added, the test passes.

> ***Note**: If a basic (non-wait state) I/O or memory cycle time is greater that 700nS, the wait bit test will be bypassed.*

4.2.7 Reset Test - Test 7

The Reset Test tests the RESET signal. RESET will be forced low, then high. The status will be verified through the PCCtest's status register.

4.2.8 Card Voltage Test - Test 8

The Card Voltage Test utilizes the PCCtest's internal A/D converter. The A/D converter is capable of measuring Vcc, Vpp1 and Vpp2. Vcc is measured with a 5% tolerance. An optional switch allows 10% tolerance for Vcc. Vpp1 and Vpp2 can usually be set to two or three levels. Software switch options allow the test to be configured for the appropriate Vpp configurations.

Switch	Name	Description
-c	Common Vpp	Vpp1 and Vpp2 on host tied together
-p	Two level Vpp	Vpp only capable of 5V and 12V levels. Otherwise three level (0V, 5V and 12V)
-t	10% Vpp tolerance	Vpp checked to 10% tolerance (Not recommended)
-w	10% Vcc tolerance	Vcc checked to 10% tolerance (Not recommended)

Table 4.2-1 Voltage Measurement options

***Note**: When common Vpp option selected, both Vpp1 and Vpp2 will be tested.*

4.2.9 Audio Out Test - Test 9

The audio out test utilizes the PCCtest internal 1KHZ audio generator. A 1 second 1KHZ burst will be placed on the -SPKR signal to test the host system's speaker circuit. The **-q** option disables the Audio Out test.

4.2.10 Test Coverage Table - 16-bit Tests

Pin	Name	Description	Test	Pin	Name	Description	Test
1	GND	Ground		35	GND	Ground	
2	D3	Data Bit 3	2,3,13	36	CD1#	Card Detect 1	
2,3	D4	Data Bit 4	2,3,13	37	D11	Data Bit 11	2,3
4	D5	Data Bit 5	2,3,13	38	D12	Data Bit 12	2,3
5	D6	Data Bit 6	2,3,13	39	D13	Data Bit 13	2,3
6	D7	Data Bit 7	2,3,13	40	D14	Data Bit 14	2,3
7	CE1#	Card Enable 1	2,3,13	41	D15	Data Bit 15	2,3
8	A10	Address Bit 10	4	42	CE2#	Card Enable 2	2,3,13
9	OE#	Output Enable	2,3,13	43	VS1	Voltage Sense 1	
10	A11	Address Bit 11	4	44	IORD#	I/O Read Strobe	2,3,13
11	A9	Address Bit 9	4	45	IOWR#	I/O Write Strobe	2,3,13
12	A8	Address Bit 8	4	46	A17	Address Bit 17	4
13	A13	Address Bit 13	4	47	A18	Address Bit 18	4
14	A14	Address Bit 14	4	48	A19	Address Bit 19	4
15	WE#	Write Enable	2,3,13	49	A20	Address Bit 20	4
16	READY IREQ#	Ready/Busy Interrupt Request	5	50	A21	Address Bit 21	4
17	VCC	Card Power	11	51	VCC	Card Power	11
18	VPP1	Programming Supply Voltage 1	11	52	VPP2	Programming Supply Voltage 2	11
19	A16	Address Bit 16	4	53	A22	Address Bit 22	4
20	A15	Address Bit 15	4	54	A23	Address Bit 23	4
21	A12	Address Bit 12	4	55	A24	Address Bit 24	4
22	A7	Address Bit 7	4	56	A25	Address Bit 25	4
23	A6	Address Bit 6	4	57	VS2	Voltage Sense 2	
24	A5	Address Bit 5	4	58	RESET	Card Reset	7
25	A4	Address Bit 4	4	59	WAIT#	Extend Bus Cycle	6
26	A3	Address Bit 3	4	60	INPACK#	Input Port Acknowledge	
27	A2	Address Bit 2	4	61	REG#	Register Select	4,13
28	A1	Address Bit 1	4	62	BVD2/ SPKR#	Battery Voltage Detect 2 Speaker	5,12,13
29	A0	Address Bit 0	4	63	BVD1/ STSCHG#	Battery Voltage Detect 1 Status Change	5
30	D0	Data Bit 0	2,3	64	D8	Data Bit 8	2,3
31	D1	Data Bit 1	2,3	65	D9	Data Bit 9	2,3
32	D2	Data Bit 2	2,3	66	D10	Data Bit 10	2,3
33	WP/ IOIS16#	Write Protect	5,13	67	CD2#	Card Detect 2	
34	GND	Ground		68	GND	Ground	

5.0 Common Problems

This section will describe some of the common problems encountered while trying to use the PCCtest socket tester on a known good host socket.

Interference with Card or Socket Services - Card and Socket Services must be disabled for the PCCtest unit to work correctly. The PCCtest software must have full control over the socket controller hardware. Do not run the PCT450 or TESTCB software in a Windows 95/98 DOS box. Boot-up in a safe mode MSDOS mode to ensure that all users of high memory area are disabled.

Interference with EMS drivers - EMS drivers may use upper memory resources that conflict with the PCCtest software. PCCtest requires the memory range from D000:0 to D7FFH during the test. Refer to your EMS driver documentation for information on excluding this memory range. Check your BIOS setup or use the -jsxxxx option to select another memory window.

Interference from Core Logic BIOS shadowing - Make sure that your core logic is not shadowing high memory in the range from D000:0 to D7FF:0. Check your EMS setup or use the -jsxxxx option to select another memory window.

Socket Controller Test Fails - Socket controller not found. If this test fails, no further testing is possible. There are several possible problems:

1. User did not specify the correct socket
2. User did not specify the correct socket controller ID (with the -bxx switch)
3. Multiple CardBus Socket controllers in system, use the -sx option to specify socket controller.

***Note**: The PCCtest unit does not need to be inserted for the Socket Controller test to pass.*

Basic Test Fails - The basic test attempts simple I/O and memory read/write patterns. A failure here will prevent further testing. A failure on a known good socket can be cause by the following:

1. PCCtest unit not inserted into the correct socket.
2. Non-standard socket controller
3. Card and Socket Services enabled
4. EMS driver allocating D000:0 memory space.
5. Chipset setup shadowing D000:0 memory space.

Vpp tests fail - There are several configurations for Vpp control in existence. In most cases the -bxx option configures the correct Vpp switching method. In applications where a non-standard Vpp switching matrix is used, the **-c, -p, -t** options should be able to configure the software for your particular configuration. See section 2.8 for a discussion of Vpp and Vcc tests.

Basic Test Failures - Card Power not being applied - Verify that the appropriate CardBus or PC Card-16 configuration header has been installed. If using the PCCtest 455, insure that the parallel port connector is properly installed and the 15 pin I/O connector is firmly seated in the PCCtest 450/460. If power is still not applied, insure that the correct -bxx option has been selected for the socket controller chip. If your are testing the TI PCI12xx/14xx/44xx series of socket controllers, refer to Appendix C for additional information. Also check to see if sufficient memory resources are available to the test. Use the –jsxxxx or –jLyyyyyyyy option to specify alternate I/O spaces.

PCCtest not receiving proper power-on reset - The PCCtest 450/460 uses it's own internal reset circuit. In order for the PCCtest to see a proper reset, the Vcc level must be below 0.1V when slot power is removed. If Vcc is greater than 0.1V when the PCCtest unit is inserted and power is off, then verify that the CardBus signals are pulled up to the switched slot Vcc, not system Vcc. The only four signals that should be pulled up to system Vcc should be CD1-, CD2-, VS1 and VS2.

Signal Quality Problems - These problems usually appear as address pattern or data pattern test failures. These problems can appear as random or pattern related. See section 5.1 for more information on signal quality issues.

Using the Wrong PCCtest Software - For 16-bit testing use the PCT450.EXE program. For CardBus testing use TESTCB.EXE.

Slot 0 fails and Slot 1 passes (CardBus tests) - If slot 0 is being used a ZV port, insure that the signal lines are kept short between the socket and Video controller. If the signals are long or there are no isolating buffers between the ZV port and the PC Card slot there may be signal quality problems.

Slot 0 fails and Slot 1 passes (CardBus tests) – During the CardBus test, the TESTCB software will assign slot 0 to PCI Bus 2 and slot 1 to PCI Bus 3. If your system has multiple PCI to PCI bridges, there may be a conflict with this assignment. The –kx option allows the user to specify which PCI bus is assigned to slot 0 and 1.

BIOS initialization of socket controller registers – Most of the newer CardBus controller have several programmable I/O pins. These pins control such functions as Zoomed Video control bits, interrupt type, activity LEDs and power control. These I/O pins are controlled by internal registers and are hardware design specific. They must be configured by the system BIOS or other software prior to running any of the PCCtest 450 software.

5.1 Signal Quality and Noise Problems

A very common problem with the PC Card interface is related to noise and signal quality. The large number of simultaneously switching signals creates a large load on the ground and power pins. Socket controller vendors try to reduce the problem through slew rate limiting and double-bonding of power pins. The designer must use proper grounding and signal conditioning techniques to insure that the interface complies with the PC Card specification. The PC Card Specification states that the interface signals remain within 0.0 volts and Vcc+0.25 volts.

One of the most common signal quality problem is over and under shoot on the interface signals. The PC Card Specification dictates that the maximum Vih be no higher than Vcc+0.25 volts and the Vil be no lower than -0.3volts. Operation beyond these limits often times cause unreliable and unexpected errors with the PCCtest series of socket testers.

Why the problem? CMOS I/O pins are clamped against Vcc and Ground through protection diodes. When the input voltage exceeds Vcc, the Vcc protection diode will start conducting. The current induced through this clamping action may be quite high (depending on the magnitude over Vcc or below ground). This current may effect adjacent logic areas and cause unpredictable failures.

The PCI and CardBus clocks must be clean and symmetric. Check the quality of the clock signals at the PCI clock input to the CardBus socket controller and at the socket.

Caution: Do not ignore these failures. While many PC cards are tolerant of such over and undershoots, many are not.

Note: For updated support information, go to the Sycard Technology website at **http://www.sycard.com**

Appendix A - 16-bit PC Card Interface

PC Card Pinout - Memory Mode

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	35	GND	Ground
2	D3	Data Bit 3	36	CD1#	Card Detect 1
3	D4	Data Bit 4	37	D11	Data Bit 11
4	D5	Data Bit 5	38	D12	Data Bit 12
5	D6	Data Bit 6	39	D13	Data Bit 13
6	D7	Data Bit 7	40	D14	Data Bit 14
7	CE1#	Card Enable 1	41	D15	Data Bit 15
8	A10	Address Bit 10	42	CE2#	Card Enable 2
9	OE#	Output Enable	43	VS1#	Voltage Sense 1
10	A11	Address Bit 11	44	RFU	Reserved
11	A9	Address Bit 9	45	RFU	Reserved
12	A8	Address Bit 8	46	A17	Address Bit 17
13	A13	Address Bit 13	47	A18	Address Bit 18
14	A14	Address Bit 14	48	A19	Address Bit 19
15	WE#	Write Enable	49	A20	Address Bit 20
16	READY	Ready/Busy	50	A21	Address Bit 21
17	VCC	Card Power	51	VCC	Card Power
18	VPP1	Programming Supply Voltage 1	52	VPP2	Programming Supply Voltage 2
19	A16	Address Bit 16	53	A22	Address Bit 22
20	A15	Address Bit 15	54	A23	Address Bit 23
21	A12	Address Bit 12	55	A24	Address Bit 24
22	A7	Address Bit 7	56	A25	Address Bit 25
23	A6	Address Bit 6	57	VS2#	Voltage Sense 2
24	A5	Address Bit 5	58	RESET	Card Reset
25	A4	Address Bit 4	59	WAIT#	Extend Bus Cycle
26	A3	Address Bit 3	60	RFU	Reserved
27	A2	Address Bit 2	61	REG#	Register Select
28	A1	Address Bit 1	62	BVD2	Battery Voltage Detect 2
29	A0	Address Bit 0	63	BVD1	Battery Voltage Detect 1
30	D0	Data Bit 0	64	D8	Data Bit 8
31	D1	Data Bit 1	65	D9	Data Bit 9
32	D2	Data Bit 2	66	D10	Data Bit 10
33	WP	Write Protect	67	CD2#	Card Detect 2
34	GND	Ground	68	GND	Ground

PC Card 16 Pinout - I/O Mode

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	35	GND	Ground
2	D3	Data Bit 3	36	CD1#	Card Detect 1
3	D4	Data Bit 4	37	D11	Data Bit 11
4	D5	Data Bit 5	38	D12	Data Bit 12
5	D6	Data Bit 6	39	D13	Data Bit 13
6	D7	Data Bit 7	40	D14	Data Bit 14
7	CE1#	Card Enable 1	41	D15	Data Bit 15
8	A10	Address Bit 10	42	CE2#	Card Enable 2
9	OE#	Output Enable	43	VS1#	Voltage Sense 1
10	A11	Address Bit 11	44	IORD#	I/O Read Strobe
11	A9	Address Bit 9	45	IOWR#	I/O Write Strobe
12	A8	Address Bit 8	46	A17	Address Bit 17
13	A13	Address Bit 13	47	A18	Address Bit 18
14	A14	Address Bit 14	48	A19	Address Bit 19
15	WE#	Write Enable	49	A20	Address Bit 20
16	IREQ#	Interrupt Request	50	A21	Address Bit 21
17	VCC	Card Power	51	VCC	Card Power
18	VPP1	Programming Supply Voltage 1	52	VPP2	Programming Supply Voltage 2
19	A16	Address Bit 16	53	A22	Address Bit 22
20	A15	Address Bit 15	54	A23	Address Bit 23
21	A12	Address Bit 12	55	A24	Address Bit 24
22	A7	Address Bit 7	56	A25	Address Bit 25
23	A6	Address Bit 6	57	VS2#	Voltage Sense 2
24	A5	Address Bit 5	58	RESET	Card Reset
25	A4	Address Bit 4	59	WAIT#	Extend Bus Cycle
26	A3	Address Bit 3	60	INPACK#	Input Port Acknowledge
27	A2	Address Bit 2	61	REG#	Register and I/O select enable
28	A1	Address Bit 1	62	SPKR#	Digital Audio Waveform
29	A0	Address Bit 0	63	STSCHG#	Card Status Changed
30	D0	Data Bit 0	64	D8	Data Bit 8
31	D1	Data Bit 1	65	D9	Data Bit 9
32	D2	Data Bit 2	66	D10	Data Bit 10
33	IOIS16#	IO Port is 16-bits	67	CD2#	Card Detect 2
34	GND	Ground	68	GND	Ground

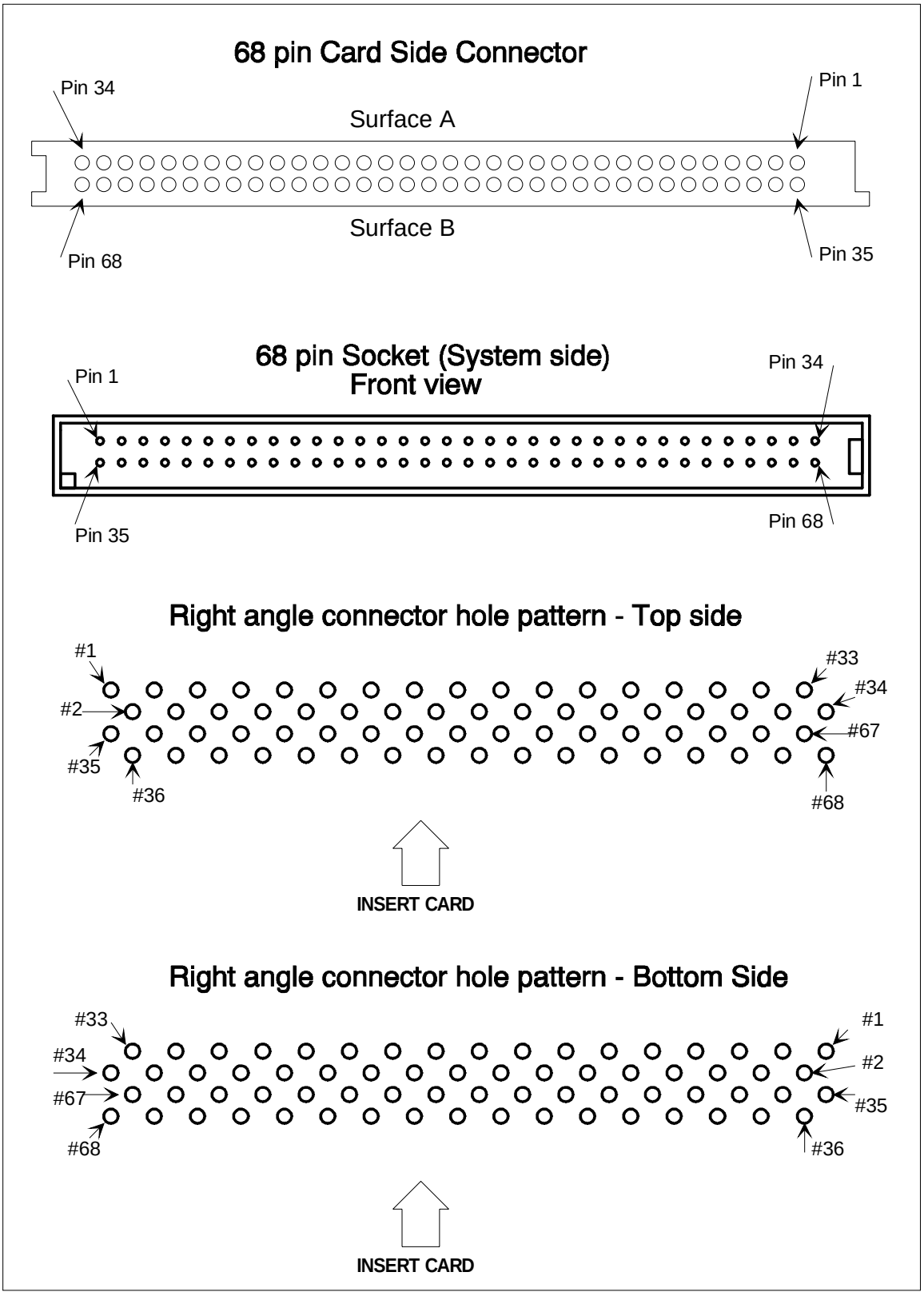
CardBus Pinout

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	35	GND	Ground
2	CAD0	ADDR/DATA 0	36	CCD1#	Card Detect 1
3	CAD14	ADDR/DATA 14	37	CAD2	ADDR/DATA 2
4	CAD3	ADDR/DATA 3	38	CAD4	ADDR/DATA 4
5	CAD5	ADDR/DATA 5	39	CAD6	ADDR/DATA 6
6	CAD7	ADDR/DATA 7	40	RFU	Reserved
7	CC/BE0#	Command/BE 0	41	CAD8	ADDR/DATA 8
8	CAD9	ADDR/DATA 9	42	CAD10	ADDR/DATA 10
9	CAD11	ADDR/DATA 11	43	CVS1	Voltage Sense 1
10	CAD12	ADDR/DATA 12	44	CAD13	ADDR/DATA 13
11	CAD14	ADDR/DATA 14	45	CAD15	ADDR/DATA 15
12	CC/BE1#	Command/BE 1	46	CAD16	ADDR/DATA 16
13	CPAR	Parity	47	RFU	Reserved
14	CPERR#	Parity Error	48	CBLOCK#	Bus Lock
15	CGNT#	Grant	49	CSTOP#	Stop/Abort
16	CINT#	Interrupt	50	CDEVSEL#	Device Select
17	Vcc	Vcc	51	Vcc	Vcc
18	VPP1	VPP1	52	VPP2	VPP2
19	CCLK	Clock	53	CTRDY#	Target Read
20	CIRDY#	Initiator Ready	54	CFRAME#	Frame
21	CC/BE2#	Command/BE 2	55	CAD17	ADDR/DATA 17
22	CAD18	ADDR/DATA 18	56	CAD19	ADDR/DATA 19
23	CAD20	ADDR/DATA 20	57	CVS2	Voltage Sense 2
24	CAD21	ADDR/DATA 21	58	CRST	Reset
25	CAD22	ADDR/DATA 22	59	CSERR#	System Error
26	CAD23	ADDR/DATA 23	60	CREQ#	Request
27	CAD24	ADDR/DATA 24	61	CC/BE3#	Command/BE 3
28	CAD25	ADDR/DATA 25	62	CAUDIO#	Audio
29	CAD26	ADDR/DATA 26	63	CSTSCHG	Status Change
30	CAD27	ADDR/DATA 27	64	CAD28	ADDR/DATA 28
31	CAD29	ADDR/DATA 29	65	CAD30	ADDR/DATA 30
32	RFU	Reserved	66	CAD31	ADDR/DATA 31
33	CCLKRUN#	Clock Run	67	CCD2#	Card Detect 2
34	GND	Ground	68	GND	Ground

Zoomed Video Pinout

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	35	GND	Ground
2	D3	Data Bit 3	36	CD1#	Card Detect 1
3	D4	Data Bit 4	37	D11	Data Bit 11
4	D5	Data Bit 5	38	D12	Data Bit 12
5	D6	Data Bit 6	39	D13	Data Bit 13
6	D7	Data Bit 7	40	D14	Data Bit 14
7	CE1#	Card Enable 1	41	D15	Data Bit 15
8	HREF	Horizontal Sync	42	CE2#	Card Enable 2
9	OE#	Output Enable	43	VS1#	Voltage Sense 1
10	VSYNC	Vertical Sync	44	IORD#	I/O Read Strobe
11	Y0	Luma Bit 0	45	IOWR#	I/O Write Strobe
12	Y2	Luma Bit 2	46	Y1	Luma Bit 1
13	Y4	Luma Bit 4	47	Y3	Luma Bit 3
14	Y6	Luma Bit 6	48	Y5	Luma Bit 5
15	WE#	Write Enable	49	Y7	Luma Bit 7
16	READY	READY	50	UV0	Chroma Bit 0
17	VCC	VCC	51	VCC	VCC
18	VPP1	VPP1	52	VPP2	VPP2
19	UV2	Chroma Bit 2	53	UV1	Chroma Bit 1
20	UV4	Chroma Bit 4	54	UV3	Chroma Bit 3
21	UV6	Chroma Bit 6	55	UV5	Chroma Bit 5
22	SCLK	Audio SCLK	56	UV7	Chroma Bit 7
23	MCLK	Audio MCLK	57	VS2#	Voltage Sense 2
24	RSVD	Reserved	58	RESET	Card Reset
25	RSVD	Reserved	59	WAIT#	Extend Bus Cycle
26	A3	ADDR Bit 3	60	LRCLK	Audio LRCLK PCM Signal
27	A2	ADDR Bit 2	61	REG#	Register and I/O select enable
28	A1	ADDR Bit 1	62	SDATA	Audio PCM Data
29	A0	ADDR Bit 0	63	BVD1	Battery Voltage 1
30	D0	Data Bit 0	64	D8	Data Bit 8
31	D1	Data Bit 1	65	D9	Data Bit 9
32	D2	Data Bit 2	66	D10	Data Bit 10
33	PCLK	Pixel Clock	67	CD2#	Card Detect 2
34	GND	Ground	68	GND	Ground

Appendix B - Connector Drawings



Appendix C - Testing the Texas Instruments PCI12xx, PCI14xx, PCI16xx, PCI15xx, PCI45xx, PCI44xx and PCI75xx Controllers

Texas Instrument's latest series of socket controllers supports a serial controlled voltage switch to control the Vcc and Vpp to the PC Card socket. Three signal lines, DATA, CLOCK and LATCH are used to control the outputs of the voltage switch. On TI's PCI12xx/14xx/44xx demo boards, the CLOCK is configured as an output from the socket controller. However, in some implementations the CLOCK signal is externally generated and is an input to the PCI12xx socket controller. A control bit in PCI configuration space address 80H called P2CCLK (Bit 27) enables the voltage switch clock output (CLOCK) from the CardBus controller chip. CLOCK is derived from the PCI clock. In the original PCCtest software, this bit was set to enable CLOCK as an output. This was required for the PCI12xx/14xx demo boards. Designs that have an externally generated CLOCK will see two sources driving the CLOCK signal when running the PCCtest software.

The latest version of the PCCtest 450/460 software supports either an externally or internally generated voltage switch clock (CLOCK) signal. The user of the PCCtest software can specify this via a command line switch. By adding a "B" suffix to the "-B6x" switch, the user specifies that the voltage switch clock is internally generated from the PCI clock.

Command line for external voltage switch clock:

TESTCB -B65 -v -0

Command line for internally generated voltage switch clock:

TESTCB -B65B -v -0

The following software revisions support this new scheme.

TESTCB.EXE Version 2.04 and above

PCT450.EXE Version 1.16 and above

ZVTEST.EXE Version 1.06 and above

PCT270.EXE Version 1.53 and above

PCT250.EXE Version 1.53 and above

